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PLEASE DELIVER TO EXAMINER STEVEN HO YIN LOKEDocket No. BUR920030102US1 (IBU-10-5802)Applicant(s): Reynolds et al

Serial No.	Filing Date	Examiner	Group Art Unit
<u>10/731,296</u>	<u>December 9, 2003</u>	<u>Steven Loke</u>	<u>2811</u>

Invention:

FPGA BLOCKS WITH ADJUSTABLE POROSITY PASS THRU

I hereby certify that this AMENDMENT is being transmitted via facsimile to the United States Patent and Trademark Office.

Fax. No. 703-872-9306

on

Nov. 30, 2004
(Date)8

(No. of pages)

TO: Examiner Loke

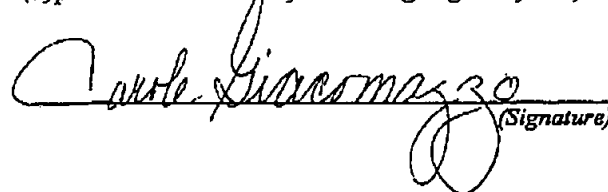
Attached is an amendment being filed in response to your Office action (restriction requirement) of November 17, 2004.

It is not believed that any fees are required. However, the Commissioner is hereby authorized to charge payment of fees associated with this communication, or credit any overpayment, to Deposit Account No. 09-0457.

FROM: James A. Lucas
CUSTOMER NO. 26681

Carole Giacomazzo

(Typed or Printed Name of Person Signing Certificate)


(Signature)

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of Reynolds et al)	Examiner: Steven Ho Yin Loke
)	
Serial No. 10/731,296)	Art Unit 2811
)	
Filed: December 9, 2003)	Confirmation No. 3650
)	
For: FPGA BLOCKS WITH ADJUSTABLE)	
POROSITY PASS THRU)	

Docket No. BUR920030102US1 (IBU-10-5802)

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Responsive to the Examiner's Office action of November 17, 2004, it is respectfully requested that the claims be amended as shown on the attached sheets. Specifically, applicants are responding to the Examiner's restriction requirement, and are electing to prosecute in the subject application Group 1 claims 1-20, drawn to a semiconductor chip.

BUR920030102US1 (IBU-10-5802)